TSMC-01-1457

December 17, 2003

To: Commissioner for Patents
P.O.Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, N.Y. 12603

Subject: | Serial No. 10/672,403 09/26/03 |

Ta-Chin Lin et al.

ALGORITHMS TUNNING FOR DYNAMIC LOT DISPATCHING IN WAFER AND CHIP PROBING

INFORMATION DISCLOSURE STATEMENT

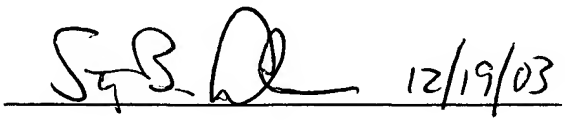
Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2003.

Stephen B. Ackerman, Reg.# 37761

Signature/Date  12/19/03

U.S. Patent 6,256,548 to Lin, "Method for Controlling Lots Dispatches of Tool Groups," discloses a method for controlling lots dispatches of tool groups.

U.S. Patent 5,841,677 to Yang et al., "Method and Apparatus for Dispatching Lots in a Factory," discloses a method for dispatching lots in a factory.

U.S. Patent 5,612,886 to Weng, "Method and System for Dynamic Dispatching in Semiconductor Manufacturing Plants," discloses a method for dynamic dispatching lots in a factory.

U.S. Patent 5,950,170 to Pan et al., "Method to Maximize Capacity in IC Fabrication," discloses a method to maximize throughput of a group of multiprocess machines whereby the number of each kind of machine is determined.

U.S. Patent 5,889,673 to Pan et al., "Manufacturing Method and System for Dynamic Dispatching of Integrated Circuit Wafer Lots," discloses a process control of manufacturing of integrated circuit (IC) chips.

U.S. Patent 5,721,686 to Shahraray et al., "Method and Apparatus for Control and Evaluation of Pending Jobs in a Factory," discloses a system and method for optimizing the scheduling of jobs in a factory.

U.S. Patent 5,546,326 to Tai et al., "Dynamic Dispatching Rule That Uses Long Term Due Date and Short Term Queue Time to Improve Delivery Performance," discloses a dynamic dispatching method for delivery performance by a factory.

U.S. Patent 5,818,716 to Chin et al., "Dynamic Lot Dispatching Required Turn Rate Factory Control System and Method of Operation Thereof," discusses how a dispatching algorithm named "Required Turn Rate (RTR)" functions according to the level of current wafers in process (WIP) algorithm revising the due date for every lot to satisfy the demand from Master Production Scheduling (MPS).

U.S. Patent 5,751,580 to Chi, "Fuzzy Logic Method and System for Adjustment of Priority Rating of Work in Process in a Production Line," discusses in a manufacturing control system for computer control of work flow in an automatic manufacturing production line with a plurality of work stations at which the progress of work is monitored, prioroty ratings are assigned to each lot ow WIP materials with the priority ratings ranging from low to high.

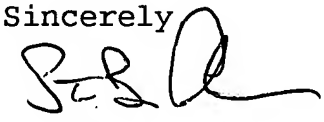
U.S. Patent 5,748,478 to Pan et al., "Output Management of Processing in a Manufacturing Plant," discloses scheduling systems for fabrication and manufacturing plants for the fabrication of integrated circuts.

U.S. Patent 5,826,238 to Chen et al., "Daily Target Generation and Machine Allocation with Priority," discloses a method and system for operating a data processing system including a data base computer system and a resource allocation computer for control of resource allocation in a manufacturing plant with a manufacturing line.

U.S. Patent 6,256,550 to Wu et al., "Overall Equipment Effectiveness On-Line Categories System and Method," discloses a manufacturing control and reporting method/system for manufacture of semiconductor devices.

U.S. Patent 5,696,689 to Okumura et al., "Dispatch and Conveyer Control System for a Production Control System of a Semiconductor Substrate," discusses a production control system applied to a process for manufacturing semiconductor substrates.

Sincerely



Stephen B. Ackerman,
Reg. No. 37761

Form PTO-1449

INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(Use several sheets if necessary)

OIPE JC56 DEC 24 2003 PATENT & TRADEMARK OFFICE

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Docket Number (Optional)	Application Number
TSMC-01-1457	10/672,403
Applicant: Ta-Chin Lin et al.	
Filing Date: 09/26/03	Group Art Unit

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	6256548	7/3/01	Lin	700	121	5/8/98
	5841677	11/24/98	Yang et al.	364	569	5/21/97
	5612886	3/18/97	Weng	364	468.07	5/12/95
	5950170	9/7/99	Pan et al.	705	7	4/11/97
	5889673	3/30/99	Pan et al.	364	468.03	12/27/96
	5721686	2/24/98	Shahraray et al.	364	468.08	10/31/96
	5546326	8/13/96	Tai et al.	364	552	4/4/95
	5818716	10/6/98	Chin et al.	364	468.06	10/18/96
	5751580	5/12/98	Chi	364	468.07	7/26/96
	5748478	5/5/98	Pan et al.	364	468.05	3/17/97
	5826238	10/20/98	Chen et al.	705	8	4/2/96

FOREIGN PATENT DOCUMENTS

	DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	Translation YES	Translation NO

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to the applicant.

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	6256550	7/3/01	Wu et al.	700	121	8/7/98
	5696689	12/9/97	Okumura et al.	364	468.28	11/27/95

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